ABSTRACT OF THE DISCLOSURE

An SPU (image processor) 12 includes: a plurality of defective pixel correction circuits each for correcting a color component signal associated with a defective pixel of an image sensor in accordance with a control signal; an input control circuit for receiving defect correction data transferred from a memory at a time of input of a plurality of color component signals; and a timing generator for generating the control signal based on the defect correction data. The defective pixel correction circuits correct color component signals associated with one and the same defective pixel in parallel, at the same time in accordance with the control signal.